IN THE SPECIFICATION:

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with strikethrough.

Please AMEND the paragraph beginning at page 1, line 23, as follows:

Further, in the computer system, it is also necessary to synchronize resources (for example, a processor and an I/O device, or, processors which are connected by a network), which usually operate asynchronously of each other, for the purpose of performing communication and the like.

Please AMEND the paragraph beginning at page 2, line 6, as follows:

Generally, when control flow branches to the interrupt service which is out of the intrinsic instruction execution order (which is denoted as a program), executing instructions are interrupted and canceled by hardware. Therefore, a "recovery" operation for removing effect of the instruction which is interrupted (or canceled) and a "restart" operation for rerunning the instruction which is interrupted are performed.

Please AMEND the paragraph spanning pages 2-3, as follows:

A pipeline method and a superscalar method are adopted as a control method for executing a plurality of instructions simultaneously in order to improvingimprove performance of a computer system. In such a control method, since interrupts may occur simultaneously in a plurality of instructions, following processes are necessary for realizing the precise interrupt.

Please AMEND the paragraph beginning at page 9, line 4, as follows:

The interrupt control circuit 49 writes an instruction address indicating a return address from the interrupt into the PCSR 39, writes a state before interrupt into the EPSR 41, and writes a state of the computer corresponding to the interrupt into the PSR 43 on the basis of interrupt notification provided from the instruction reading control part 9 or the instruction execution part 5. A branch address corresponding to the occurred interrupt is provided to the program counter 13.